

REMARKS

Claims 46-63 are added by this amendment. Claims 44-63 are pending in the application.

Claims 44 and 45 stand rejected under 35 U.S.C. § 112, 2ND ¶, as being indefinite. Claims 44 and 45 have been amended to address the concerns noted in the Office Action, but these amendments do not change the scope of the claims. The Office Action alleges that it is confusing that the capacitors may be made by any method at all but that the "lateral spacing" dimension is defined only for those capacitors made using a photolithographic step.

Capacitors used in integrated circuits, such as DRAMs, are used in conjunction with a broad variety of other components, including interconnections, diodes, transistors, resistors etc. Typically, at least some of these components are created using photolithography. Photolithographic processes include a minimum photolithographic feature dimension. Accordingly, the capacitors may be formed using any process at all but their dimensions and separation may be defined in terms of other elements taken from the context where the capacitors are employed, or may be defined in terms of photolithographic constraints applicable to formation of the capacitors.

The Office Action also states that "minimum photolithographic feature dimension" is indefinite, because one cannot determine what this dimension might be without reference to a process of making, and no

1 process of making is specified. The specification provides exemplary
2 processes in conjunction with the embodiments of Figs. 1-12, 13-16
3 and 17-21, along with associated text.

4 Applicants are not required to exhaustively list all possibilities,
5 rather, the requirements of 35 U.S.C. § 112, 1ST ¶ include that the
6 specification sets forth the best mode contemplated by the inventor for
7 carrying out the invention (see MPEP 2106, §V(B)). The Office Action
8 offers the opinion that “one cannot claim a feature size that varies over
9 time” but fails to provide any authority for this opinion.

10 The language “minimum photolithographic feature dimension” refers
11 to a definite and well-known characteristic of photolithographic processes
12 in concrete terms well and long understood by those having any skills
13 in the relevant arts. The Office Action poses rhetorical examples of
14 what might be a minimum photolithographic feature dimension, and
15 inquires as to which is applicable. The smallest of these feature
16 dimensions, as determined by a photolithographic process, would logically
17 be the minimum.

18 Claims 44 and 45 stand rejected under 35 U.S.C. § 112, 1ST ¶,
19 as containing subject matter which was not described in the specification
20 in such a way as to reasonably convey to one skilled in the art that the
21 inventor had possession of the claimed invention at the time the
22 application was filed. The Office Action maintains that the claims thus
23 attempt to encompass processes that would be used in the future.

1 Applicants note that every patent claim ever filed is directed to actions
2 by an infringer in the future. The requirements that the applicant needs
3 to meet in order to have a valid claim are spelt out in detail in 35
4 U.S.C. § 112, 1ST ¶.

5 These requirements are (i) that the specification provides a written
6 description of the invention (see pp. 4-13 of the specification as filed)
7 and (ii) that the specification sets forth the best mode contemplated by
8 the inventor for carrying out the invention. Applicants have met these
9 requirements.

10 The fact that the invention may be used in combination with other
11 steps and processes is irrelevant (see MPEP 2106, esp. §§V(A)2 and
12 (B)). When the claimed capacitors are fabricated in conjunction with
13 some photolithographic process used to form an integrated circuit, that
14 process will include a minimum photolithographic feature dimension as
15 a standard and well-understood characteristic of that process.

16 Claims 44 and 45 stand rejected under 35 U.S.C. § 102(b) as
17 being anticipated by Morihara et al., "Disc-Shaped Stacked Capacitor Cell
18 For 256 Mb Dynamic Random-Access Memory", Jpn. J. App. Phys.,
19 Vol. 33, No. 8, pp. 14-19 (1994). Applicants disagree and request
20 reconsideration.

21 Morihara et al. teach away from the invention as recited in
22 claims 44 and 45, stating (1ST ¶, 3RD sentence) that "In the case of
23 a 256 Mb DRAM of which cell area is $0.72 \mu\text{m}^2$, a simple stacked

1 capacitor (STC) cannot be used to obtain sufficient capacitance.”
2 Morihara et al. further teach away from the claimed subject matter by
3 noting (3RD ¶) that “In fin structures, sufficient capacitance is achieved
4 by increasing the number of storage nodes: however, the layout area of
5 the storage node is limited by the photolithographic process.”

6 Claim 45 further distinguishes by reciting that the stem has a
7 minimum width which is less than the minimum photolithographic feature
8 dimension. Morihara et al. describe a stem that is formed using a
9 photolithographic step (see § 3, description of Fig. 2A) and that thus
10 has a minimum dimension no smaller than the minimum
11 photolithographic feature dimension. Further, Morihara et al. do not
12 describe fins projecting laterally from a stem, as recited in claim 45.
13 For at least these reasons, claims 44 and 45 are allowable over the cited
14 reference.

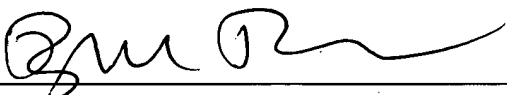
15 New claims 46-63 describe structures of the capacitors in more
16 detail and are allowable. New independent claims 49 and 56 describe
17 the subject matter of claims 44 and 45, but with some differences in
18 scope. New claims 46-63 are supported by text appearing at pages 4-13
19 of the specification as filed.

20 In view of the foregoing, allowance of claims 44-63 is requested.
21 The Examiner is requested to phone the undersigned in the event that
22 the next Office Action is one other than a Notice of Allowance. The
23

undersigned is available for telephone consultation at any time during
normal business hours (Pacific Time Zone).

Respectfully submitted,

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By: 
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